UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,939	11/08/2001	Sheila M. Rader	CS11241	4806

23125 7590 04/08/2004

MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
7700 WEST PARMER LANE MD: TX32/PL02
AUSTIN, TX 78729

EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	4

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,939	RADER, SHEILA M.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-18 and 20-25* is/are rejected.

7)☒ Claim(s) *4, 12 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on November 18, 2001.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 2 and 10 recite the limitation "the first and second memory controllers" in lines 2- There is insufficient antecedent basis for this limitation in the claim.

5. Claims 3 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what is meant by SRAM/SDRAM or Flash/ROM. Does the Applicant mean SRAM or SDRAM and Flash or ROM memory? Clarification is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Zhao (PGPUB: US 2003/0105906).

Ware discloses a virtual channel memory controller (Figures 27 and 31, Controller); a first memory device (Figure 27, Reference 2703) coupled to the virtual channel memory controller by a dedicated first bus (Figure 27, Reference 2708); a second memory device (Figure 27, Reference 2730) coupled to the virtual channel memory controller by a dedicated second data bus (Figure 27, Reference 2747); a shared address and control bus interconnecting the virtual channel memory controller and the first and second memory devices (Figure 31, Reference 3107). Ware does not explicitly disclose a DSP and RISC processor and a display controller coupled to virtual channel memory controller via a first DMA and second DMA channel respectively on a single integrated circuit, synchronous memory devices and a wireless communication system comprising the above features. Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Thus, it would have been obvious to one of ordinary skill in the art to use a SDRAM in Ware's system for increased speed and improved performance. Additionally, Zhao discloses a wireless communication system (Figure 9, Reference 5) comprising a DSP (Figure 9, Reference 10B) and RISC processor (Figure 9, Reference 10A) coupled via a first and second DMA channel respectively to a memory controller (Figure 9, Reference 15) and a display controller (Figure 9, Reference 16) coupled to the memory controller on a single integrated circuit (Figure 9, Reference 1). Memory systems are not stand-

alone systems. They are used to store information for another device and thus it is evident that Ware's system is used in some type of processing system. Wireless system provides long-range communication with other systems at high data speeds and hence it would have been obvious to one of ordinary skill in the art to use Ware's system in a wireless communication system, such as the system taught by Zhao, for the desirable purpose of high speed and long-range communication.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Zhao (PGPUB: US 2003/0105906) as applied to claim 1 and further in view of Nain (USPN: 5,978,866).

Ware and Zhao do not disclose the virtual memory channel controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus. However, Nain teaches the concept of a memory controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus (Figure 3, References 112 and 114; C 7, L 9-19). These features taught by Nain ensure proper operation of the bus via the arbitration logic and proper directing of information to a device from the shared bus via the multiplexer. It would have been obvious to one of ordinary skill in the art to include these features in the system taught by Ware and Zhao for the desirable purpose of accuracy and to ensure proper bus operations.

9. Claims 9, 11, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311).

Ware discloses a virtual channel memory controller (Figures 27 and 31, Controller); a first memory device (Figure 27, Reference 2703) coupled to the virtual channel memory controller by a dedicated first bus (Figure 27, Reference 2708); a second memory device (Figure 27, Reference 2730) coupled to the virtual channel memory controller by a dedicated second data bus (Figure 27, Reference 2747); a shared address and control bus interconnecting the virtual channel memory controller and the first and second memory devices (Figure 31, Reference 3107). Ware does not explicitly disclose the memory devices as synchronous memory devices. Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Thus, it would have been obvious to one of ordinary skill in the art to use a SDRAM in Ware's system for increased speed and improved performance.

Regarding claim 17, Ware does not explicitly disclose maintaining a state of the shared bus during an interval between addressing the first and second synchronous memory devices, however, it is well known in the art to maintain a state of a bus until the time when the state of the bus changes. For example, during a reset all signals and buses are set to a known state until such time when the state changes. Inherently this process reduces power because the state of the line being high or low does not transition to other state. Hence, it would have been obvious to one of ordinary skill in the art to include this feature in the system taught by Ware for the desirable purpose of reducing power consumption.

10. Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Nain (USPN: 5,978,866).

Ware does not disclose the virtual memory channel controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus. However, Nain teaches the concept of a memory controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus (Figure 3, References 112 and 114; C 7, L 9-19). These features taught by Nain ensure proper operation of the bus via the arbitration logic and proper directing of information to a device from the shared bus via the multiplexer. It would have been obvious to one of ordinary skill in the art to include these features in the system taught by Ware for the desirable purpose of accuracy and to ensure proper bus operations.

11. Claims 14-15 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Haba et al. (PGPUB: US 2001/0053069).

Ware discloses the limitations cited above, however, Ware does not disclose concurrently accessing the first and second synchronous memory devices. However, Haba teaches the concept of concurrently accessing memory devices (Page 7, Section 0104; Page 13, Section [0169-0170]; Page 22, lines 3-8). This feature taught by Haba improves the performance of the system by increasing the throughput of the memory. Hence, it would have been obvious to one

of ordinary skill in the art to use Haba's teachings with the system taught by Ware for the desirable purpose of improved performance.

12. Claims 16, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Nakaoka (USPN: 6,021,077).
Ware discloses the limitations cited above, additionally Ware discloses accessing the first and second memory but not while addressing one of the first and second synchronous memory devices. Nakaoka teaches the concept of addressing a memory while accessing the memory (Figure 9, refer to clock cycles C7 – C9). This feature provides fast access to the memory and thus further improves the performance of the system. Hence, it would have been obvious to one of ordinary skill in the art to use Nakaoka's teachings with the teachings of Ware for the desirable purpose of improved performance.

13. Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311).
Ware discloses a virtual channel memory controller (Figures 27 and 31, Controller); a first memory device (Figure 27, Reference 2703) coupled to the virtual channel memory controller by a dedicated first bus (Figure 27, Reference 2708); a second memory device (Figure 27, Reference 2730) coupled to the virtual channel memory controller by a dedicated second data bus (Figure 27, Reference 2747); a shared address and control bus interconnecting the virtual channel memory controller and the first and second memory devices (Figure 31, Reference

3107). Ware does not explicitly disclose the memory devices as synchronous memory devices nor does Ware disclose a wireless communication system comprising the features stated above. Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Thus, it would have been obvious to one of ordinary skill in the art to use a SDRAM in Ware's system for increased speed and improved performance. Memory systems are not stand-alone systems. They are used to store information for another device and thus it is evident that Ware's system is used in some type of processing system. Wireless system provides long-range communication with other systems at high data speeds and hence it would have been obvious to one of ordinary skill in the art to use Ware's system in a wireless communication system, such as the system taught by Zhao, for the desirable purpose of high speed and long-range communication.

Regarding claim 25, Ware does not explicitly disclose maintaining a state of the shared bus during an interval between addressing the first and second synchronous memory devices, however, it is well known in the art to maintain a state of a bus until the time when the state of the bus changes. For example, during a reset all signals and buses are set to a known state until such time when the state changes. Inherently this process reduces power because the state of the line being high or low does not transition to other state. Hence, it would have been obvious to one of ordinary skill in the art to include this feature in the system taught by Ware for the desirable purpose of reducing power consumption.

Allowable Subject Matter

14. Claims 4, 12 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

April 5, 2004